



Direct Bond Interconnect (DBI™)

Scalable Technology Platform For High-Performance 3D ICs

Semiconductor technology at 65nm and below is plagued by high drive currents, long interconnect delays and poor yields. Ziptronix DBI technology offers a better solution to designers of mixed-signal, high-performance systems.

DBI combines a room or low temperature, non-adhesive covalent bonding technique with integrated high-density interconnect formation. DBI makes possible 3D circuits and tiled wafers with the highest performance and lowest cost available, for silicon, III-V or other materials. Unlike other 3D fabrication methods, no wire bonding, solder bumping or pressure are required, and through-silicon vias eliminate large-area design exclusions.

DBI begins with chemical-mechanical polishing (CMP) to planarize the surfaces of the materials to be bonded. The CMP also exposes the respective buried interconnect connection points, or Through Silicon Via (TSV). Following CMP, a thin layer of silicon oxide (SiO_2) is applied to both surfaces, which are aligned so the Supercontacts points will meet. The oxide is activated to create a direct spontaneous covalent bond formation. It exceeds the fracture strength of the bonded materials.

The bond energy between the surfaces is very high and brings the Through Silicon Via (TSV) into contact close to each other to form effective electrical connections. Their low resistance enables better power efficiency and reduces the overall power consumption of the 3D system. Because the process is completed at room or low temperature, there are no residual stresses, such as can occur with thermal or anodic bonding methods, nor are there epoxies or other materials that require curing. The bond also is hermetic.

Direct Bond Interconnect (DBI™)

Available Now

The patented, proven DBI technology is available now for licensing by foundries, IDMs, fabless IC companies and end users. Ziptronix also offers prototyping and technology-transfer services.

Benefits

- A compelling alternative to expensive, time-consuming device scaling
- Alleviates interconnect delays and reduces parasitics and power consumption, while increasing system speed and performance
- Dramatically reduces production costs (significantly less costly than thermo-compression bonding techniques)
- Uses standard fab tools, for fast technology transfer
- Each 3D tile is fabricated in its optimum “native” process (e.g. memory, digital, analog, RF, etc.)
- Bonds and interconnects mixed materials (e.g. silicon, III-V devices)
- Post-bonding thinning enables processing of full-thickness wafer and die for improved alignment accuracy and reduced stress

Features

- Interconnect pitch $\leq 10\mu\text{m}$
- Accommodates 1.5M connections/cm²
- No adhesives, solders, pressure, underfill or wire bonding required to bond and connect layers of active devices
- Uses standard fab tools and processes
- Highest reliability of all 3D processes because of hermetic sealing
- Accommodates face-to-face architectures (top die/wafer upside down)
- Accommodates face-to-back architectures (use of through-die vias/buried contacts)

Applications

- All die-to-wafer and wafer-to-wafer implementations, including 3D circuits or 2D tiles on a wafer
- Mixed-signal circuits (e.g. integrated analog/digital)
- Memory applications: stacked memory on high-speed processor; high performance SiP; memory module
- Folding of large 2D ICs into 3D stacks

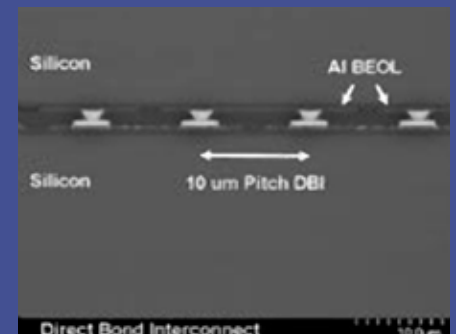
Material Preparation Requirements

- Semi-standard waviness, bow and warp
- Inert RIE to clean surfaces and enhance surface porosity
- NH₄OH exposure terminates surface with amine groups
- Bond energies > 1 J/m² obtainable at room temperature
- Oxide deposition + CMP to 0.5nm RMS spec

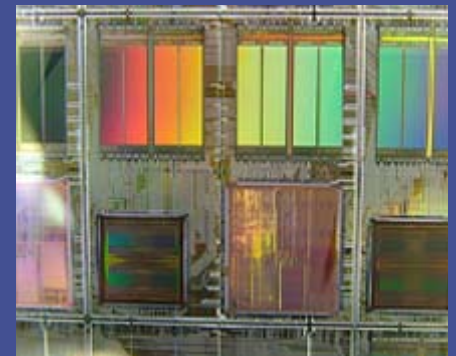
For further details on the DBI process and suitable applications, contact us at info@ziptronix.com



DBI™ pick & place placement accuracy is +/- 1μm over 3σ.



DBI technology makes possible high-density interconnect between stacked devices.



Improved performance and reliability over other stacking technologies, in the smallest profile.