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# Benefits of 3D Integration in Digital Imaging Applications

## INTRODUCTION

Digital Imaging is a platform technology driving rapid growth in consumer, industrial and aerospace product markets (Loizides, et al., 2000; Somogyi, 1999). Current single chip, imaging solutions have improved cost, power, and form factor (Herrick, Yook, & Katehi, 1998; Ronen, et al., 2001; Somogyi, 1999). However, current single chip strategies face significant constraints that affect the cost and performance of large arrays and that prevent low cost solutions in IR and UV spectral ranges (Abshire & Andreou, 2001).

This paper introduces a novel 3D digital imaging integration strategy that will revolutionize the cost and performance of imaging technology. The following sections will outline the constraints inherent in today's technology and the advantages created by the use of Ziptronix 3D integration.

## 2D ARCHITECTURE: A SERIES OF COMPRISES

When a conventional 2D silicon process is used to build an imaging chip, there are a number of trade-offs that significantly affect cost, performance, and design versatility. Generally these trade-offs result from combining several distinct functions on a single chip – conversion of the optical signal (the image) to an electrical signal followed by analog and digital processing of the electrical signal. Specific examples of the trade-off include the following:

- **Substrate Selection –** A single substrate must be chosen. This substrate must support photo conversion, analog signal processing, and digital signal processing. Considered separately each of these tasks would optimally result in different choices for the substrate. 2D approaches dictate a compromise.

- **Process Constraints –** A single process flow is used for photo conversion devices, analog circuitry, and digital circuitry. This is another significant compromise. For example color fidelity and brightness resolution require high bit count A/D conversion. In general the bit count of an A/D converter is estimated as follows:

  Maximum Signal $\cong V_{dd}$
  Minimum Signal $\cong \sqrt{{}^{kT}/_{C}} \cong 60mv@C = 1pF\ at\ 300K^{o}$
  # of Bits $= \log_2 \{ V_{dd}/\sqrt{{}^{kT}/_{C}} \}$

  It can be seen that the number of bits depends most strongly on $V_{dd}$. Thus a 16-bit A/D converter may require 3.3 volts. Yet digital processing continues to scale Vdd to lower values (2.5 volts for 0.25 micron technology, 1.8 volts for 0.18 micron technology, 1.2 volts for 0.13 micron technology.) This voltage scaling presents a fundamental problem in achieving the required dynamic range of the analog circuitry.

- **Array Efficiency –** The chip areas required for electronics (A/D conversion, amplification, clocking, etc.) are typically comparable to the areas used for photo conversion. Where possible, the electronics are placed around the photo conversion pixel array but this is not possible for pixel amplifiers, line drivers, etc. These devices and associated interconnect networks are included in the pixel array significantly compromising the array efficiency (the % of the pixel array that is photoactive) it is common for array efficiencies to be less than 50%.

- **4-Edge Buttable –** As mentioned in the discussion of array efficiency, support electronics are typically arranged around the periphery of the photo conversion array. This is a significant trade-off in that it prevents creation of large arrays by tiling smaller arrays. Ideally an imaging chip would be 4-edge buttable.

- **Spectral Range –** Except for exotic applications, single chip imaging is largely confined to Silicon-based substrate technologies. There is no low cost methodology to manufacture high resolution, single chip imagery using non-Silicon materials to extend the spectral range in the IR and UV wavelengths.

In the following section we will describe how Ziptronix “solves” each of these trade-offs.

## 3D ARCHITECTURE: FREEDOM FROM CONSTRAINTS

**Basic Approach:** Ziptronix uses a proprietary process to achieve foundry-based, wafer scale integration of separately processed “layers” of circuitry. The focused ion beam micrograph in Figure 1 shows a standard CMOS logic device integrated with an SPROM separated by the Ziptronix bond interface. In this example, the devices are connected using the existing peripheral pad rings. However, since the Ziptronix process results in true covalent bonds at the interface, direct connections can be made between layers (Figure 2) supporting direct connection between a pixel array and processing logic. Figure 3 shows an InP epitaxial stack integrated with standard CMOS logic. The ability to mix materials in 3D integration allows each critical function to be implemented in its own cost/performance-optimized process.

**Figure 1: Logic & Memory 3D integration**

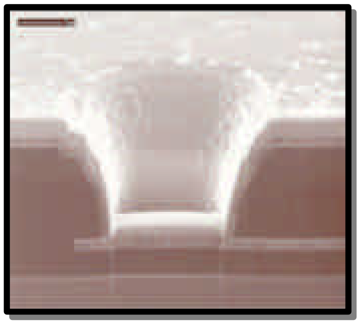

**Figure 2: 2u Via through Ziptronix bond interface**

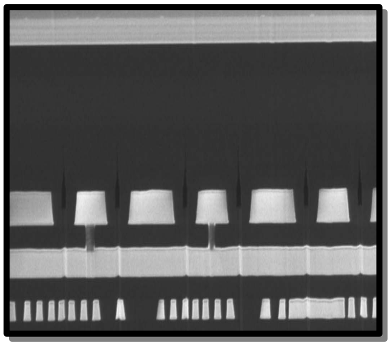

**Figure 3: InP EPI stack w/ Si**

After the wafer is integrated using the Ziptronix process, it is diced into individual 3D ICs. The interconnected memory/logic pair referenced in Figure 1 is shown in its final, pre-packaged form in Figure 4. In this photo, the memory die is shown on top and is interconnected to an FPGA array using a standard lithography and metalization flow. This 3D integration method eliminates the problems associated with conventional 2D integration, described above. Specifically,

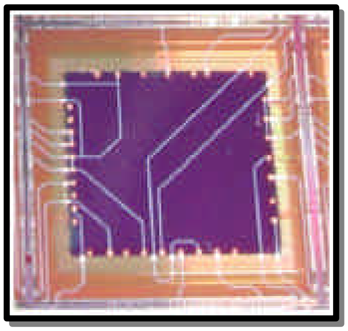

**Figure 4: Final 3D integration**

- **Substrate Selection –** Photo conversion is done in the uppermost layer. Thus substrate selection for photo conversion is independent of analog or digital functional criteria.

- **Process Constraints –** Depending on the number of layers, fabrication of the photo conversion layer (for example a CCD-based array) is completely separate from processing of the support electronics. If three layers are used processing of the support electronics may be further divided between analog and digital functions.

- **Array efficiency –** Because Ziptronix allows via-based pixel-by-pixel interconnection to the underlying electronics the array efficiency can approach 90%. In most cases this represents at least a factor of two improvements.

- **4-Edge Buttable –** The entire die area of the upper surface is devoted to photo-conversion, thus the array may be designed to be a 4 edge buttable module. Each such module may be independently tested prior to tiling. This is a huge advantage in the cost effective manufacturing of ultra high resolution, large area arrays.

- **Spectral Range –** Because the substrate selection and processing of the photo conversion layer are decoupled from the balance of system electronics there is no barrier to the use of photo converters for IR or UV applications. Note that Ziptronix technology supports both wafer to wafer and die to wafer integration. Thus materials not available at the wafer scale of Silicon may be integrated as "die" on 200 mm or 300 mm Silicon wafers. This completely changes the economics of these products, allowing them to move from exotic industrial and military applications into mainstream consumer products. Note as well that a single design for the "host" electronics can be used with a number of different photo conversion strategies. This is a huge significant saving in NRE and increases volume-based savings in wafer production.

- **Concurrent Processing –** As mentioned above, Ziptronix enables via-based pixel-by-pixel interconnection to the support electronics. This opens the door to low cost, real time photo-enhancement techniques previously only obtainable at enormous cost and after the fact. Today pixel data emerges as a serial bit stream that is routed to memory and "massaged" by a separate processor according to the desired algorithms. Ziptronix provides pixel-by-pixel parallel access to the array, thus many photo-enhancement algorithms can be enabled in real time as a parallel operation on the entire array. This is revolutionary.

## SUMMARY

This white paper outlines several major advantages created by Ziptronix based processing of 3D digital imaging chips. Ziptronix solutions can resolve key challenges in digital imaging – cost, power consumption, resolution, form factor, spectral range, and "intelligence".

## REFERENCES

Abshire, P., & Andreou, A.G. (2001). "Capacity and Energy Cost of Information in Biological and Silicon Photereceptors," Proceedings of the IEEE, vol. 89 (7), pp. 1052 – 1064.

Herrick, K.J., Yook, J.G., Katehi, L.P.B. (1998). "Microtechnology I the Development of Three-Dimensional Circuits," IEEE Transactions on Microwave Theory and Techniques, vol. 46, pp. 1832-1944.

Loizides, L., Pidgeon, B., Card, D., Allard, K., Leathern, R., McAteer, S., & Schieffelin, Z (2000). "Digital Imaging: Integrating Services to Increase Consumer Retention and Revenue," Jupiter Communications Online Intelligence, Vision Report, vol. 1.

Ronen, R., Mendelson, A., Lai, K., Lu, S., Pollack, F., & Shen, J.P. (2001). "Coming Challenges in Microarchitectrure and Architecture," Proceedings of the IEEE, vol. 89 (3), pp. 325-340.

Somogyi, S (1999). "Furture Perfect," Interactions, Nov – Dec, vol.6.