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3D Integration for Mixed Signal Applications

INTRODUCTION

Wireless products are expected to lead the recovery in electronics markets: cell phones, WLAN products, pagers, bluetooth enabled products, etc. are becoming key market drivers – this is a large change for what has long been a PC centered chip industry (Enright, 1999; Faloon, 2001; Peckham, 2001). Like the PC, these products must sustain a versioning strategy by offering a series of models that do more for less. The PC competition was a spiral of higher processor speeds and more memory *at lower cost*. Now the competition is to deliver an increasing menu of services on an anytime/anywhere basis – voice, data, location dependent services, music, video, etc. *at lower cost*. The cornerstone of anytime/anywhere is wireless connectivity, and the cornerstone of wireless is the mixed signal integrated circuit combining analog and digital functions (Bindra, 1999; Plas, et al., 2001).

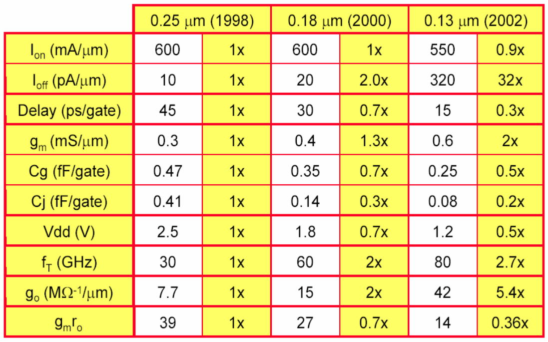
These wireless/mixed signal market opportunities pose significant problems for the IC industry (Plas, et al. 2001; Tai, 2000). The IC industry has been driven by digital applications. Design tools, design rules, foundry processes, packaging standards – in short everything from "frontend" to "backend" is geared for digital products. Many digital resources are not easily adapted to analog applications and the situation is rapidly getting worse (Plas, et al., 2001).

This white paper outlines key problems inherent in creating analog solutions from a digital process flow and shows how Ziptronix technology provides a cost effective strategy for future generations of mixed signal products.

MIXED SIGNAL APPLICATIONS – THE CHALLENGES FOR SOC

CMOS scaling is driven by digital performance considerations and economics (die yield/wafer) (Annema, 1999). Process scaling (making everything smaller) is the prime objective (Chiueh, 1992). When these scaled CMOS process flows are used for analog designs, there are significant compromises (Brodersen, et al., 2001; Gregor, 1992; Plas, et al., 2001). With each succeeding process node the compromises are more severe. This is raising questions about the viability of a large number of analog circuit topologies beyond the 130nm node. In the following section, we will consider the main implications of CMOS scaling that impact analog design for mixed signal SOCs.

CMOS – THE IMPLICATIONS OF SCALING



	0.25 µm (1998)		0.18 µm (2000)		0.13 µm (2002)	
I_{on} (mA/µm)	600	1x	600	1x	550	0.9x
I_{off} (pA/µm)	10	1x	20	2.0x	320	32x
Delay (ps/gate)	45	1x	30	0.7x	15	0.3x
g_m (mS/µm)	0.3	1x	0.4	1.3x	0.6	2x
Cg (fF/gate)	0.47	1x	0.35	0.7x	0.25	0.5x
Cj (fF/gate)	0.41	1x	0.14	0.3x	0.08	0.2x
Vdd (V)	2.5	1x	1.8	0.7x	1.2	0.5x
f_T (GHz)	30	1x	60	2x	80	2.7x
g_o ($M\Omega^{-1}/\mu m$)	7.7	1x	15	2x	42	5.4x
$g_m r_o$	39	1x	27	0.7x	14	0.36x

The above chart outlines the changes in device and operating parameters that have occurred over the past three process generations. There are three parameters that deserve special attention:

I_{off} – this combines sub-threshold leakage and gate leakage. It can be seen that leakage is rapidly increasing at a disproportionate rate.
V_{dd} – core voltages are steadily shrinking.
$G_m r_o$ – maximum gain is falling.

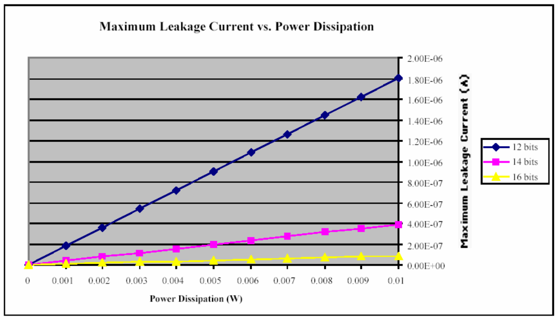
Each of these three trends has a severe negative impact on analog design as outlined in the following sections.

Leakage

Charge control circuits, such as sample and hold latches, depend on accurately holding the signal value (a voltage on a capacitor) to within ½ of the least significant bit (LSB). Leakage introduces an error voltage (Ferre & Figueras, 2002). A first order analysis allows us to quantify the power argument (Sodini, 2002). Essentially the designer must maintain the inequality, where the left hand side (LHS) is leakage, I_{off}.

$$\boxed{(I_G + I_{SUB}) < \frac{P_{Diss}}{2nV_{th}\left(2^{N+1}\right)\ln\left(2^{N+1}\right)}}$$

It is seen that as leakage increases there is only one practical option – to increase the right hand side, power dissipation. However, note that the required power dissipation has an exponential dependence on the number of bits (N). This can be seen in the following plot.



Note that the power dissipation required for 12 bits at a leakage of 1.8E-06 A is 0.01 W. At the same value of leakage the power dissipation required for 16 bits is literally "off the chart". Moreover, as discussed above, "the same value of leakage" is not the case – leakage is rapidly getting worse.

The message is clear. Future generations of CMOS cannot be used for low power, high-resolution analog applications unless leakage is controlled. Proposed fixes for gate leakage may not help analog applications. The digital problem presented by leakage is increased static power. Novel gate materials, such as hafnium oxide, that provide large *k* values may allow a thicker gate insulator thereby reducing reduce tunneling current. An analog solution is more complex. For example, to date the 1/f noise characteristics of all such novel insulators prevent their use for many analog applications.

Effect of Core Voltage Scaling on Dynamic Range

Dynamic range is primarily dependent on V_{dd} (Bamha, et al. 2001). To first order we can estimate the number of bits at a given V_{dd} as:

Maximum Signal $\cong V_{dd}$
Minimum Signal $\cong \sqrt{{}^{kT}/_{C}}$
# of Bits $= \log_2 \{ V_{dd}/\sqrt{{}^{kT}/_{C}} \}$

Plugging in values we see that for 16 bits of resolution at $V_{dd} = 1.2$ V (core voltage in the 130 nm process node) we require a minimum signal of 18 µV. This requires a well-controlled capacitance, C=11 pF, (a very large capacitance value in a 130nm process). Any increase in resolution (# of bits) or a decrease in V_{dd} will require an increase in capacitance. Unless current is similarly scaled, any increase in capacitance will result in an increase in settling time…slowing system response. At constant resolution (# of bits) and constant settling time if V_{dd} is scaled down by a factor, s, then Power must be scaled up by the same factor, s. Such power scaling offers a poor trade-off for battery powered anytime/anywhere products.

Gain Falloff with Scaled Output Resistance

Negative feedback circuits are of fundamental importance for AD/DA converters. The continued falloff of $g_m r_o$ with r_o can make these topologies unworkable.

TECHNICAL SUMMARY

CMOS scaling trends favorable to digital designs are resulting in increased leakage, loss of dynamic range and reduced gain. These factors will render the analog portion of many mixed signal designs impractical beyond 130 nm.

ECONOMIC REALITIES

Scaling Penalties: Each new generation of process technology costs more per unit area than the preceding generation. In the digital world this is more than compensated for by shrinkage of the area required for the digital circuit in the new process node. Because circuit area shrinkage dominates the rising processing cost per unit area, the net result is cheaper digital functionality (the basis for Moore's Law) Analog devices and circuits scale do not scale as favorably. Thus the rising process cost per unit area dominates and the net result is more costly analog functionality (Gregor, 1992).

Design Cost:

1. Analog design takes longer and is more uncertain than digital design (Plas, et al. 2001).
2. Analog performance is hurt by process scaling further complicating design (Tai, 2000).

In spite of scaling penalties and increasing design costs the analog portions of mixed signal designs must be redone (practically from scratch) with every revision of the digital process. This adds greatly to the cost of product revision, lengthens the time to market, and adds considerable uncertainty to the project (Gregor, 2001).

Design Reuse: While today's tools are far from perfect, digital designs are often ported to a new process or foundry. Analog design tools are much less mature/complete and analog designs are much more "locked in" to a specific process (Plas, et al., 2001). The cost of porting a mixed signal design is virtually the same as for a new design.

THE CONVENTIONAL SOLUTION – PACKAGING

SIP – System in a Package: Given the problems inherent in the use of scaled CMOS for analog design, a conventional approach is to separately process the analog and digital functions and combing the separate die in a package (Tai, 2000). This decouples design, allows the analog part to remain fixed through several digital revisions, and allows the analog function to be built in a friendly process (say a 2.5 or 3.3 Volt, 0.25 micron technology).

There are several drawbacks to this multi-die approach.

- Wafer scale economics beat die scale economics (essentially Moore's Law).
- Many of today's products like cell phones, PDAs, etc. are very sensitive to footprint/volume.
- Off chip (packaged-based) parasitics often dominate SIP performance.
- Off-chip power per unit bandwidth is orders of magnitude larger than on-chip power per unit bandwidth.
- While testing a mixed signal chip is by no means easy, it is much easier and cheaper than mixed signal testing of a multi-chip module *(Aside from purely technical considerations module test raises numerous questions of the "who owns what and when did they own it" kind).*

THE ZIPTRONIX SOLUTION – 3D MIXED SIGNAL INTEGRATION

Ziptronix offers a superior solution and a sustainable advantage. Separate process flows are used to build wafers for the analog and digital functions. These process flows are cost and performance optimized for each particular application. The separate functions may be tested at wafer scale prior to integration. Ziptronix technology is used to provide wafer-scale, foundry-based integration of digital and analog functions into a single die, 3D IC of standard thickness suitable for industry standard packaging. Such a product has all of the economic and technical benefits of a single die product – and avoids the compromises inherent in forcing an analog design into an unfriendly digital process flow.

The Ziptronix *Drop-On*™ approach to functional integration provides a natural path to design reuse. The analog layer need not be redesigned with each revision of the digital design. This allows customers to distribute the analog NRE over several product generations.

Key performance characteristic can be superior to those of a conventional 2D SOC IC. For example, a key concern in mixed signal performance is noise – particularly the effect of digital switching noise on embedded analog performance. Substrate coupling is an important mechanism for noise injection. In the Ziptronix approach, the analog substrate and digital substrate are separated with complete dielectric isolation. A separate ground plane can be provided in the metalization sequence between the layers to provide additional EMI isolation. But most importantly in contrast to the 2D SOC approach – *using Ziptronix-based 3D integration the analog function is built in an analog process.*

SUMMARY

A new 3D integration process is introduced based on Ziptronix proprietary, room-temperature, non-adhesive die-to-wafer bonding and interconnect technology.

Analog and digital devices are built in their own optimized processes and combined into a single 3D solution. Time to market and cost are reduced, as scaling and redesign efforts are no longer needed.

The Ziptronix process significantly reduces cost and footprint compared to a conventional SIP approach.

Analog circuits are now immune from design changes aimed at reducing CMOS power consumption.

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