Scalability and Low Cost of Ownership Advantages of Direct Bond Interconnect (DBI®) as Drivers for Volume Commercialization of 3-D Integration Architectures and Applications.

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Scalability and Low Cost of Ownership Advantages of Direct Bond Interconnect (DBI®) as Drivers for Volume Commercialization of 3-D Integration Architectures and Applications

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ABSTRACT

Advantages of Direct Bond Interconnect (DBI®) technology for the volume commercialization and manufacture of 3-D Integrated Circuits are described. These advantages include low cost resulting from a simplified and high-throughput tool set, scalability resulting from a planar bond surface, and heterogeneous materials integration resulting from a low thermal budget.

INTRODUCTION

3-D technology has recently emerged as a solution to relentless market demand for the simultaneous continual improvement in device cost, performance, and footprint for high volume applications like mobile, wireless and gaming [1,2]. The initial wave of implementation has utilized established packaging technologies like wirebonding, adhesives and bumping to stack die or packages. While this implementation has been successful at delivering improvements in cost, performance, and footprint, further improvements, beyond the capability of established volume production technology, will be required [3-5]. This scaling can be achieved with Ziptronix' CMOS-compatible direct oxide bond and Direct Bond Interconnect (DBI®) technology and through silicon via (TSV) technology [6]. Before these technologies will be adopted and qualified for volume manufacturing, low cost implementation and applications requiring these improvements must be established. This paper reviews applications driving the adoption of advanced, scalable 3-D technology and the suitability of Ziptronix' direct oxide bond technology for this adoption.

APPLICATIONS DRIVING ADOPTION OF SCALEABLE 3-D TECHNOLOGY

3-D technology comprises bonding, thinning, and interconnecting layers of wafers or die. The scalability of 3-D technology refers to the capability to provide the minimum thickness of and highest density of connections between these layers. Available 3-D manufacturing technology is currently based on established packaging technology that is capable of a modest interconnection density and stack thickness. The interconnection density is limited by conventional wirebonding and bumping technologies and the stack thickness is limited by the package thickness for stacked package implementations like package-on-package or die (wafer) thinning and handling for stacked die (wafer) implementations.

Advanced technologies capable of significantly increased interconnection density and reduced layer thickness have been developed and are ready for adoption [6-8]. Barriers to volume manufacturing implementation of this improved capability include the cost to install and qualify and demand of customer applications that require this capability. Emerging applications capable of establishing the requisite demand include pixilated 3-D architectures, wide low-latency memories, and 3-D SoCs.

Pixelated 3-D Architectures

Pixelated 3-D architectures have a periodic array of 3-D interconnections between the bonded 3-D layers with the minimum pixel size limited by the interconnect pitch. The die size of integrated circuits (ICs) fabricated with these architectures is proportionate to the square of the interconnection pitch for applications where the pixilated array dominate the die size. The ability to scale these applications to smaller pitch thus has the potential to greatly increase the number of good die on a wafer and provide an excellent return on the added process cost investment of a scalable 3-D technology. An example of this type of application is CMOS Image Sensors (CIS) where the pixel pitch has scaled from about five microns in 2003 to less than two microns in 2008. Further pixel pitch reductions in conventional 2-D CIS are limited by sensitivity and filter proximity to the detecting silicon [9]. A low-cost 3-D bonding technology that enables aggressive backside thinning and illumination will enable further scaling of the pixel pitch to below one micron. Future CIS architectures that require pixel-level 3-D interconnections to improve on-chip data processing, dynamic range, linearity, and power consumption will further require a 3-D interconnect scalable to sub-micron pitch.

Wide, Low-Latency Memories

Traditional CMOS 2-D Moore's Law scaling has resulted in ICs exceeding a billion transistors, ten levels of interconnect and 10 GHz clock speed. There are numerous challenges to improving this performance by extrapolating 2-D scaling. One of the most significant challenges is the power consumption required to switch this quantity of transistors and drive the interconnect at the desired rate. This problem is exacerbated by the need to keep processors fed with memory. Notwithstanding processor ICs with over 80% of the area dedicated to on-chip L1 and L2 cache, applications require considerable access to off-chip main memory. This memory access is narrow and requires the transfer of blocks with more data than required by the processor. Processor ICs have moved to multi-core processors to improve performance without further increases in clock rate and power consumption. However, the effectiveness of this approach is limited by code that can be efficiently implemented in parallel threads.

3-D allows a significant improvement in this memory access bottleneck by providing memories that are wider and can be intimately connected to a processor IC resulting in reduced latency and power consumption. The wider memories have been developed with a multi-layer 3-D wafer-to-wafer bonding technology with Super-Via™ TSVs and 3-D interconnects with a sub-ten microns pitch. The multi-layer stacking with fine pitch interconnect allows a 3-D memory architecture capable of built-in self-test and built-in self-repair for higher yields and lower test cost [7]. These wider memories can also be 3-D integrated directly onto processor ICs to enable a much lower access to memory than can be achieved compared to conventional off-chip solutions [10].

3-D System-on-Chip

Conventional 2-D System-on-Chip (SoC) has earned significant market by providing for increased functionality on a single piece of silicon. However, increased IC size, additional mask levels, and restrictions imposed by building in a single node have limited the yield, cost, and performance of this solution.

A 3-D SoC avoids these limitations by enabling the partitioning of a 3-D SoC into distinct layers that can be built in optimized nodes and yield curves [11]. The realization of these ICs will require 3-D design tools. Although some 3-D design tools have recently become available, CMOS foundries will need to adopt 3-D process technology and develop 3-D process design kits with these tools and process technologies before 3-D SoCs will become generally available and their advantages achieved. Pixelated architectures and memories that require less of this infrastructure are thus more likely to drive volume manufacturing adoption of advanced 3-D process technology.

DIRECT BOND TECHNOLOGY

Direct bonding refers to the ability to bond surfaces, for example silicon oxide surfaces by placing them in intimate contact without a different material at the bond interface to facilitate the bonding. Historically, achieving an adequate bond strength required high temperatures (> 600 °C) after the surfaces were contacted to convert weak hydrogen Van der Waals forces to strong covalent bonds [12]. The requirement of a high temperature has caused some to refer to this as fusion bonding, implying a melting and significant mass transport across the bond interface.

Low-Temperature Direct Bond Technology

Low-temperature direct bond technology is a direct bond technology developed by Ziptronix that is capable of achieving very high bond energies between two smooth surfaces at low temperatures that are required for a number of high volume applications like 3-D CMOS ICs [13]. The technology is compatible with a variety of surfaces including silicon, silicon oxide, and silicon nitride. A number of patents have been granted that protect the technology [14-19]. Key strengths of the Ziptronix technology include the ability to implement this technology in a wide variety of ambient conditions, for example by activating, then terminating the surfaces before bonding. A variety of surface activations and terminating species is possible. This process is generic in a way that it is effective with a wide variety of dielectrics including oxides and nitrides, deposited or grown by a variety of techniques including thermal, physical vapor deposition, TEOS, and high-density plasma. The process can be used to bond virtually any two materials together, in particular when a dielectric can be deposited on the material and polished if necessary. It is also very effective bonding a dielectric to silicon.

The specific surface activation and termination for a specific pair of surfaces results in particular kinetics of the bond energy after the surfaces are placed together. An example of these kinetics for a dry inert RIE process and wet ammonia rinse is given in Figure 1 where it is shown that a bond energy in excess of 4 J/m^2 can be achieved at 250 °C. The bond energy can continue

to increase for times longer than that shown in Figure 1. For example, a bond energy in excess of 1.5 J/m^2 at room temperature can be achieved after 18 days. This capability of the process can be enabling when bonding materials with a very high coefficient of thermal expansion (CTE) mismatch that requires a very high bond energy before any heating to avoid shearing of the bond.

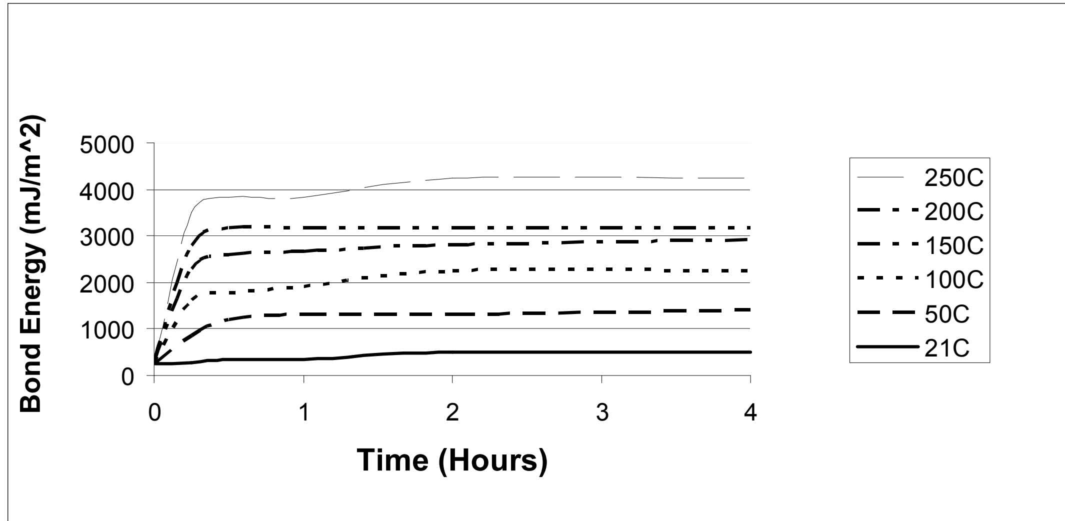

Figure 1 – Bond energy in mJ/m^2 as a function of time in hours and temperature after bonding silicon oxide surfaces that have been reactive ion etched activated and ammonia terminated.

Direct Bond Interconnect (DBI®) Technology

Direct Bond Interconnect (DBI®) is a patented technique whereby electrical interconnections are formed across a direct bond interface [20, 21]. This can be achieved by first forming two planar heterogeneous surfaces, each comprised of insulating and conductive portions, where the conductive portions can be electrically connected to circuitry below the surface. These planarized surfaces are then aligned with opposed insulating and conductive surfaces, and placed together. When silicon oxide is used as the insulating portion and metal as the conductive portion, a direct bond is formed between opposed silicon oxide surfaces and an electrical interconnection across the bond interface results from a direct metallic bond formed between opposed metal surfaces. A direct bond between misaligned insulating and conductive surfaces can also form. The result is a planarized bond interface traversed with electrical interconnections. The planar surfaces can be formed with a variety of processes including etch / fill / polish (i.e., damascene), or electroplate / oxide deposition / polish. The use of planar surfaces allows very small sub-micron pitch electrical interconnections to be formed. An example of sub-micron structures surfaces that can be formed with a damascene process include tungsten and copper plugs used in volume manufacturing today. Scanning electron micrograph cross-sections of a 3.0 and 1.5 micron pitch redundant daisy chain link built with an electroplate / oxide deposition / polish process are given below in Figures 2 and 3, respectively. Note the bond

interface with distinct metallic grain structure on either side of the bond interface, indicative of a direct, non-fused bond.

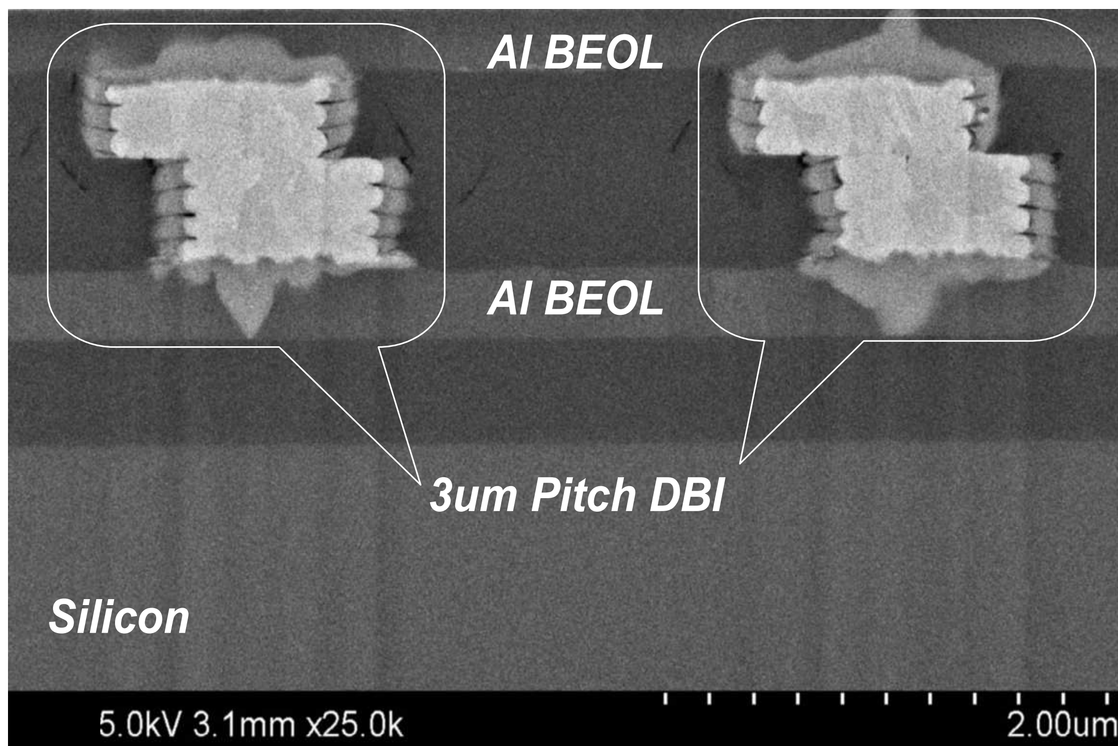

Figure 2 – Scanning electron micrograph of two DBI® connections in a four-fold redundant, 3.0 micron pitch, daisy chain link.

Very high bond energies at low or room temperature can be obtained after bonding by using the Ziptronix CMOS-compatible direct bond technology described above. The metal interconnections can also be formed at low or room temperature if the surface metallic oxide prior to bonding is non-existent, negligible or conductive. If the surface metallic oxide is not negligible, low-resistance electrical interconnections can be obtained by heating the bonded structure after a high bond strength has been achieved between opposed insulating portions at low temperature. The difference in coefficient of thermal expansion between the insulator and metal that results generates significant internal pressure at the bond interface to overcome the native oxide and result in a low resistance interconnect. Figures 2 and 3 give an example of this scenario using silicon oxide as the insulator and nickel as the metal where the low-resistance interconnect is achieved at 300 °C. This process is currently available for prototyping at Ziptronix with or without redundant connections at a standard pitch of 50, 25, 10, and 8 microns. Alternate metals and their alloys including, but not limited to, copper, tungsten, nickel, indium, indium-tin-oxide, and gold are also good candidates for DBI®. The development of non-redundant connections at 3 and 1.5 micron pitch and alternate DBI® metals is in progress.

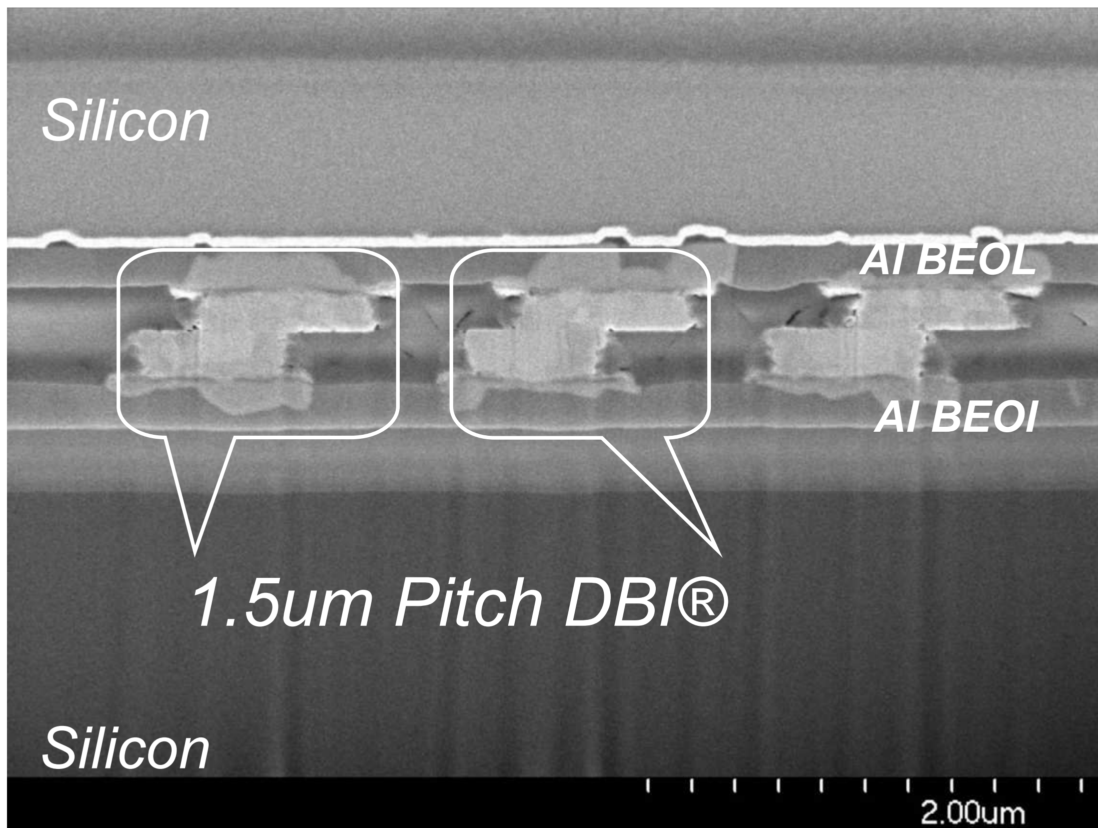

Figure 3 – Scanning electron micrograph of three DBI® connections in a nine-fold redundant, 1.5 micron pitch, daisy chain link.

DIRECT OXIDE BOND AND DBI® TECHNOLOGY ADVANTAGES

A variety of advantages of the Ziptronix DBI® 3-D interconnect technology include low cost of ownership, scalability, heterogeneous integration, and reliability.

Cost of Ownership

The cost of ownership (CoO) in a volume semiconductor manufacturing process is principally determined by the cost of the process tools and the throughput of wafers in these tools. In a bonding process, the cost of the tool used to align, place and bond wafers and the throughput of die or wafers through this tool are thus critically important to the CoO of the bond process. Wafer bonding tools typically include a bond chamber to execute the bonding portion of the process. This bond chamber adds cost and can be a throughput bottleneck for some bond processes like copper thermo-compression. The Ziptronix CMOS-compatible direct bond and DBI® processes are fundamentally low CoO in this regard in that they do not require a bond chamber that can significantly increase the CoO. An example of the potential cost savings that

can be achieved was recently provided by Yole [22] where a savings of $45 from $57 to $12 was projected by eliminating an expensive, low-throughput bond chamber.

Eliminating the need for a bond chamber is also advantageous for achieving high throughput die-to-wafer implementations of 3-D technology. (Die-to-wafer implementations are required for the highest volume 3-D applications due to the lower cost that can result from use of known-good-die, mismatched die size, and mismatched wafer size.) For example, low-cost, high-throughput pick-and-place tools can be used to align and place wafers when using the Ziptronix direct bond technologies.

Another cost advantage of the Ziptronix technology is provided by the high, uniform bond strength across the entire bond interface that enables thinning of bonded layers after bonding and thinning to submicron scale. The ability to thin after bonding avoids thin wafer handling CoO. Thinning to submicron scale allows minimizing TSV depth which is a significant cost driver in 3-D implementation.

Scalability

The Ziptronix DBI® technology offers optimum 3-D scalability with regard to the highest density of 3-D interconnections and the thinnest layering. This scalability is enabled by the inherent planarity and high, uniform bond strength of the technology.

The importance of planarity in scalability has been repeatedly proven by conventional CMOS, for example with tungsten and copper plugs. The ultimate 3-D interconnection scaling limit using DBI® is thus expected to be determined by the accuracy of alignment and placement tools. The ability to accurately pattern without run-out across 300mm (450mm) wafers may also be a limiting factor for wafer-to-wafer applications. The recent announcements of wafer-to-wafer alignment tools with accuracies less than 0.3 microns is consistent with the expectation that sub-micron 3-D interconnect pitches will soon be available.

The high, uniform bond strength across the entire insulating and conductive bond interface enables the technology to be relatively insensitive to misalignment compared to other technologies like copper thermo-compression. It also allows the realization of very thin layers, for example micron thick epitaxial layers that enable the fabrication of Symmetric Intrinsic Heterojunction Bipolar Transistors ICs [23].

Heterogeneous Integration

3-D applications requiring heterogeneous integration are likely to become of increasing importance due to the increased functionality they offer. Examples of heterogeneous integration can be categorized as functional, for example analog, digital, memory, MEMs, optical, etc. or material, for example silicon, GaAs, InP, GaN. Both types of heterogenous integration can require low thermal budgets after integration. For example, the heating of programmed memory after integration can result in erasure of critical information required for functionality. Integrated materials with mismatched CTE can also have a limited thermal budget to avoid breaking of the material with temperature variation. The Ziptronix technology has proven to be very robust in this regard by enabling the bonding of very highly mismatched material combinations like fused silica to lithium tantalate [24].

Reliability

The very high bond strength offered by the Ziptronix direct bond and DBI® technologies is indicative that the technology is fundamentally reliable. For example, bond energies well in excess of the silicon fracture energy (2.5 J/m^2) are readily obtained that results in the silicon substrate breaking before the bond when using the technology to build 3-D CMOS ICs. The reliability of the DBI® connections has also been proven in a number of test structures and prototypes built with the technology. Accelerated moisture resistance (JEDEC HAST standard) and temperature cycling tests of daisy chains with 1,000,000 serial connections have not resulted in failure of the DBI® interface, even after three times the standard storage time and ten times the number of cycles.

CONCLUSIONS

Direct oxide bonding and Direct Bond Interconnect (DBI®) are ideally situated for adoption as a 3-D integration volume manufacturing technology due to their advantages of low cost, scalability and heterogeneous integration.

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