Low Cost of Ownership Scalable Copper Direct Bond Interconnect 3D IC Technology for Three Dimensional Integrated Circuit Applications

P. Enquist, G. Fountain, C. Petteway, A. Hollingsworth, and H. Grady
Ziptronix, Inc., Morrisville, NC, 27560
Email: p.enquist@ziptronix.com   Tel: (919) 459-2456

Keywords – Bonding, Direct Oxide Bonding, Non-Adhesive Bonding, Molecular Bonding, Direct Metal Bonding, Direct Copper Bonding, Direct Bond Interconnect, Direct Internal Metal Thermo-Compression Bonding, Fine Pitch 3D Interconnect, Heterogeneous Integration, Reliability.

Abstract

This paper presents preliminary results of a copper–based Direct Bond Interconnect (DBI®) 3D integration process that has been developed to leverage foundry standard copper dual damascene and Ziptronix bond technology to achieve scalable, very low Cost-of-Ownership, 3D interconnects with minimum foundry adoption barrier. Results achieved include 100% operable arrays of 72,500 3D copper DBI® interconnections on a 25 micron pitch with a 125°C thermal budget and 10 micron pitch 3D copper DBI® interconnections with a 350°C thermal budget. DBI® contact resistance and resistivity achieved are about 50 mohm / connection and < 0.45 ohm/um^2, respectively, using 4 micron diameter Cu DBI® plugs and a TiW barrier layer. Reliability results include bare die that pass temperature cycling and HAST JEDEC tests.

Introduction

Three dimensional integrated circuits (3D ICs) are well known for increased performance resulting from reduced signal delays and power consumption. Adoption of this technology for volume semiconductor manufacturing will require other aspects of scalability, specifically cost reduction, to be realized.

There is significant potential for manufacturing cost reduction by building ICs in 3D from 2D strata because partitioned strata can be independently optimized for cost, yield, functionality, and die size [1]. Optimizing realization of this cost reduction will require implementation of a 3D IC technology with a lowest Cost-of-Ownership (CoO).

It is also vital that a 3D integration technology that scales laterally and vertically be implemented. Lateral scalability will allow the highest density of 3D interconnections between two adjacent 2D IC strata within a 3D IC that will enable micron scale pitch 3D interconnect applications required for pixilated architectures in applications like image sensing and displays. Vertical scalability will enable micron scale 2D IC strata thickness required for 3D heterogeneous integration of 2D strata with significant coefficient of thermal expansion (CTE) mismatch and highest 3D density memory stacking.

Direct Bond Interconnect (DBI®) is a 3D IC process technology that has been invented, developed, and pioneered by Ziptronix, Inc. for lowest 3D IC CoO and highest density of 3D interconnections and stacking by achieving a direct or non-adhesive bond between two planarized and aligned arrays of interconnections on opposed die or wafer surfaces. The technology is covered by a number of Ziptronix patents, e.g., [2].

DBI® is a member of the family of technologies shown in Figure 1 that provide a 3D interconnect in conjunction with a bond between two adjacent 2D IC strata within a 3D IC. These technologies have the advantage of not requiring a via etch and fill process to interconnect the 2D IC strata that would otherwise consume valuable silicon in one of the strata and preclude scaling [3,4]. Within this family of technologies, DBI® has the advantage of the highest and most uniform bond strength capability that enables superior lateral 3D interconnect and vertical strata scaling. Companies who have reported results using this technology include Ziptronix, Inc. [5-8] and CEA Leti [9].

The inherent uniform bond strength capability of DBI® results from a direct or non-adhesive bond component with insulating material that is laterally disposed relative to a conductive bond component that provides the integral 3D interconnect as shown in Figure 2.

The conductive bond component can be metallic or non-metallic and if metallic, can be ,but is not limited to, direct metal-to-metal, direct internal metal thermo-compression with or without grain growth, or solder reflow. The conductive bond can be realized simultaneously with or separately from the direct insulative bond. For example, if the conductive bond is direct metal-to-metal and the bond surfaces are suitably planar and activated/terminated, the direct insulative and conductive bonds can be realized in the same process step. Alternatively, if the conductive bond is direct metal internal thermo-compression, the conductive bond can be realized in a heat treatment after and facilitated by the direct insulative bond as a result of internal compression of the conductors resulting from adequate insulator bond strength and the CTE mismatch of the insulator and metal.

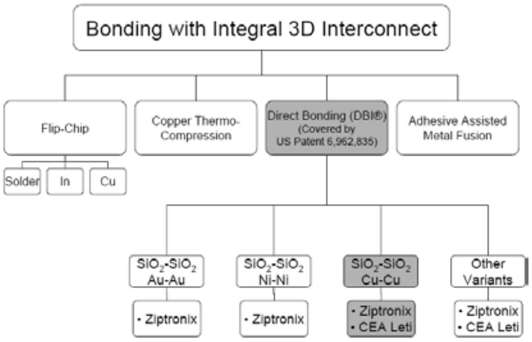


Figure 1 – Family tree of 3D IC bond technologies with an integral 3D interconnection, including companies who have reported results using Direct Bond Interconnect (DBI®) technology. Shaded branch is the primary subject of this work.

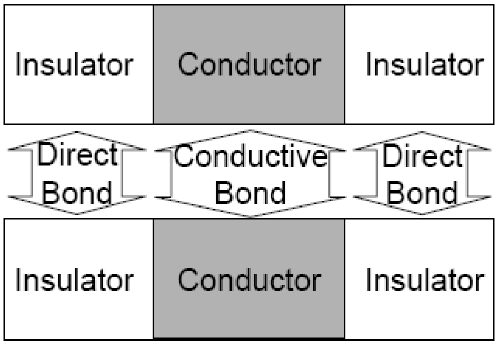


Figure 2 – DBI® cross-sectional schematic showing direct or non-adhesive insulative bond component laterally disposed relative to a conductive bond enabling a uniform and high strength 3D interconnect bond.

The inherent low CoO capability of DBI® technology is enabled by a high direct bond energy at high throughput ambient manufacturing conditions that eliminates the need for relatively low throughput, expensive tools to align, place, and bond 2D IC wafers or die together. These CoO advantages of the DBI® technology have been independently and quantitatively verified [10].

Among the earliest demonstrations of DBI® capability have been results reported by Ziptronix, Inc. using direct or non-adhesive silicon oxide insulative bonding and gold metal direct [5] or nickel internal thermo-compression [6-8] bonding. Scalability to 1.5 micron pitch (> $4x10^7$ 3D interconnections /cm^2), 10^6 yielded 3D interconnections per part, and reliability exceeding JEDEC standards have been achieved. These non-limiting embodiments of DBI® used a type of direct or non-adhesive silicon oxide bond that achieves characteristically high bond energies at low temperatures after bond surfaces have been activated, terminated, aligned and placed into contact. This bond technology and its low thermal budget capabilities has been pioneered, extensively developed, trademarked as ZiBond™ and is covered by a number of patents, e.g., [11-17]. Both ZiBond™ and DBI® technologies have been released and are available for licensing [18].

The nickel DBI® implementation at Ziptronix, Inc. was achieved with the planarization of arrays of nickel filled vias or plugs in a silicon oxide matrix resulting in high yield 3D interconnections after a 300°C post-insulative bond anneal [6-8]. Although nickel is a good solution for a wafer level packaging supply chain implementation or integration with DRAM foundry nickel TSV [19], alternate metals like aluminum, tungsten, and copper may be preferred for other foundry implementations like aluminum or copper back-end-of-line (BEOL). Furthermore, some applications, for example certain types of 3D memory and heterogeneous integration, require a thermal budget < 300°C.

P. Gueguen, et. al, have recently reported DBI® results using copper direct or thermo-compression bonding [9]. Single connections with a connection resistance of 0.98 Ohm/um^2 after a 200°C heat treatment on a pitch of about 300 microns were achieved.

This work reports on an advanced version of copper DBI® available from Ziptronix, Inc., with superior 10 micron pitch, < 0.5 Ohm/um^2 connection resistance, 125°C thermal budget, 72,500 serial daisy chain 3D interconnection yield, and dual damascene integration with a barrier layer.

Approach

The ideal copper DBI® process will be easy to integrate into existing foundry copper dual damascene BEOL, operable with existing foundry tools and within manufacturable control limits, and not materially increase the CMOS thermal budget.

The industry standard copper BEOL key process steps include dielectric deposition, via and trench etch, conductive copper diffusion barrier liner, copper electroplated or PVD fill, copper CMP, and silicon nitride cap. The last copper metal layer in the multi-layer BEOL interconnect stack is typically capped with an aluminum pad to facilitate packaging. The copper CMP process step is ideal for integration with the copper DBI® process as it leverages the existing manufacturing toolset and process capability. The two obvious options for copper DBI® integration are after copper CMP of the copper filled trench in the standard dual damascene process or after copper CMP of a copper filled via in a single damascene copper via process as shown in Figure 2. The initial implementation of copper DBI® was with a copper via CMP because of the similarity to established nickel DBI® CMP processes and the potential to realize the most scalable 3D interconnect.

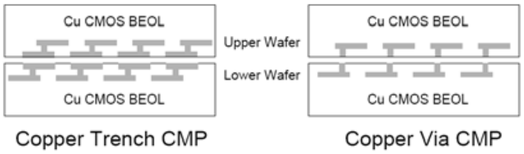


Figure 3 – Cross-sectional schematics of two aligned copper trench and via CMP wafers before DBI® bonding.

The nickel DBI® CMP process [6-8] was developed using industry standard CMP tools, pads and slurries to facilitate technology transfer to a volume semiconductor foundry manufacturing environment. Likewise, the approach taken to develop the copper DBI® process reported here was to use these same tools and consumables. Relative to nickel DBI® CMP, achieving a stable copper DBI® CMP process was expected to be more challenging due to increased chemical susceptibility and mechanical softness of the copper resulting in enhanced dishing consistent with that observed with copper dual damascene.

Experimental

The copper DBI® process was developed using a daisy chain built from wafers that consisted of a 1.2 micron tall copper etched and filled via in silicon oxide on top of a 0.7 micron thick copper damascene routing layer. The copper filled trench was lined with a TiW diffusion barrier and capped with a silicon nitride barrier layer, similar to that used in copper BEOL high volume manufacturing. The copper dishing was optimized and controlled within limits available to Ziptronix, Inc., licensees [18].

A version of the Ziptronix, Inc., ZiBond™, low temperature, high bond strength, silicon oxide direct or non-adhesive bond process was used as bond surface preparation prior to aligning and placing wafers into contact in a Laurier CDB-50, +/- 1 micron over 3σ accuracy pick and place tool. Nitrogen plasma activation and termination was used to avoid chemically compromising the exposed copper prior to alignment and contact placement. After contact, wafers were heated to different temperatures to evaluate the effect of heating on the copper DBI® conductive bond. After heating, all but 2-3 mils of silicon from one of the wafers was removed with a combination of backgrind and CMP. Vias to test pads were cut with photolithography and SF6 etching.

Initial process development focused on a 72,500 element, 25 micron pitch daisy chain process control monitor (PCM). After achieving fully functional 25 micron pitch PCMs, 463,000 element, 10 micron pitch daisy chain PCMs were developed. PCMs were tested with a Rucker & Kolls probe station and a HP 3478A multimeter.

Results and Discussion

Fully functional 25 micron pitch, 72,500 element daisy chain PCMs with four micron diameter Cu DBI® vias or plugs were built with a post-contact heat treatment of 125°C. The DBI® contact resistance and resistivity were about 50 mohm / connection and < 0.45 ohm/um^2, respectively. A scanning electron micrograph (SEM) cross-section of four serial copper DBI® connections of one of these daisy chains is shown in Figure 4. A higher magnification SEM cross-section of a single copper DBI® connection is shown in Figure 5. The distinct grain structure on either side of the conductive bond interface confirms a low temperature copper direct or internal thermo-compression without grain growth conductive bond.

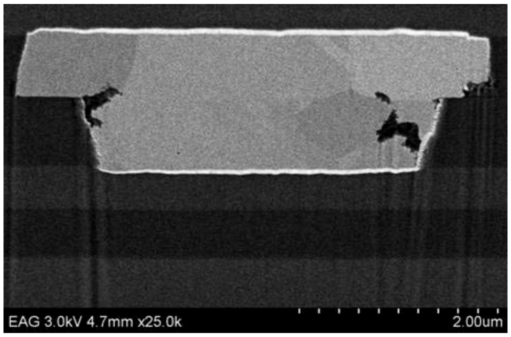


Figure 4 – Scanning electron micrograph cross-section of four copper DBI® connections of a 72,500 element, 25 micron pitch daisy chain with a 125°C heat treatment.

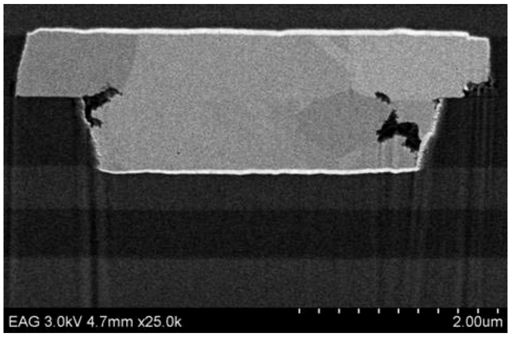


Figure 5 – Scanning electron micrograph cross-section of one copper DBI® connection of a 72,500 element, 25 micron pitch daisy chain with a 125°C heat treatment.

Fully functional 25 micron pitch, 72,500 element daisy chain PCMs were also achieved with a post-contact heat treatment of 350°C. An SEM cross-section of a single copper DBI® connection of one of these daisy chains is shown in Figure 6. The grain structure on either side of the conductive bond interface in this part is not distinct confirming an internal thermo-compression with grain growth conductive bond. No significant difference in electrical performance for the PCMs heated at temperatures between 150°C and 350°C was observed.

Daisy chain PCMs with 463,000 elements on a 10 micron pitch with three micron diameter Cu DBI® vias or plugs were also fabricated with a post-contact heat treatment of 350°C. Copper DBI® contact resistance and resistivity were comparable to that of the 25 micron pitch, 72,500 element daisy chain PCMs. An SEM cross section of four serial electrically connected copper DBI® connections from a 463,000 element daisy chain PCM is shown in Figure 7.

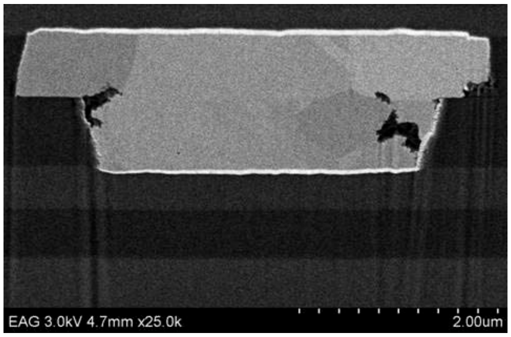


Figure 6 – Scanning electron micrograph cross-section of one copper DBI® connection of a 72,500 element, 25 micron pitch daisy chain with a 350°C heat treatment.

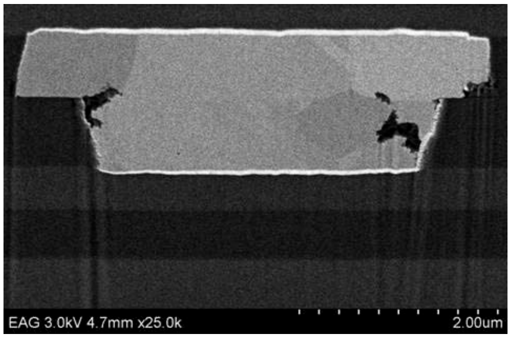
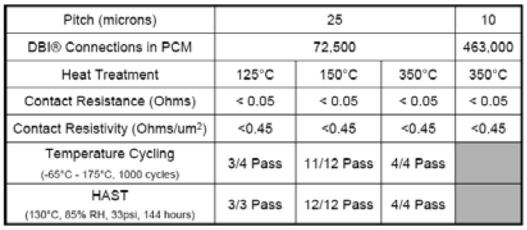


Figure 7 – Scanning electron micrograph cross-section of four copper DBI® connections of a 463,000 element daisy chain, 10 micron pitch with a 350°C heat treatment.

Singulated bare die comprised of a single copper DBI® 25 micron pitch, 72,500 element daisy chain PCM with heat treatment of 125°C, 150°C or 350°C were subjected to JEDEC temperature cycling and HAST reliability tests. Two separate sets of samples were used for HAST and temperature cycling tests. The HAST sample set had 3, 12, and 4 parts, with heat treatments of 125°C, 150°C and 350°C, respectively. The temperature cycling set had 4, 12, and 4 parts, with heat treatments of 125°C, 150°C and 350°C, respectively. A summary of these reliability results is shown in Figure 7 along with the electrical results for the 25 and 10 micron pitch daisy chain PCMs. No HAST failures were observed for any of the parts. Likewise, no temperature cycling failures were observed for the 350°C heat treatment parts. The only failures observed were for one part each of the 125°C and 150°C temperature cycling parts.



Pitch (microns)	25			10
DBI® Connections in PCM	72,500			463,000
Heat Treatment	125°C	150°C	350°C	350°C
Contact Resistance (Ohms)	< 0.05	< 0.05	< 0.05	< 0.05
Contact Resistivity (Ohms/um^2)	<0.45	<0.45	<0.45	<0.45
Temperature Cycling (-65°C - 175°C, 1000 cycles)	3/4 Pass	11/12 Pass	4/4 Pass	
HAST (130°C, 85% RH, 33psi, 144 hours)	3/3 Pass	12/12 Pass	4/4 Pass	

Figure 7 – Summary of electrical and reliability results.

The distinct grain structure on either side of the direct bond interface in the SEM cross sections of the fully functional 72,500 element, 25 micron pitch daisy chain PCMs indicates the two most likely mechanisms for formation of the conductive bond component of the copper DBI® results reported here are direct metal-to-metal or direct internal metal thermo-compression. The combination of copper filled via thickness and copper CTE relative to the silicon oxide matrix is expected to result in direct contact of the copper filled vias at about 125°C for a copper CMP dishing of about 3 nm. Less copper dishing is expected to result in significant internal thermo-compression generated by the low temperature, strong silicon oxide direct or non-adhesive ZiBond™, restricting expansion of the copper DBI®. For example, 1 nm of dishing and 125°C is expected to result in a stress with comparable percent of modulus of elasticity as that calculated for nickel DBI® at 300°C [20]. Given that the 1-3 nm of copper dishing is within the process control of the copper DBI®, it is difficult to conclude which of these two mechanisms is primarily responsible for formation of the conductive bond component of the copper DBI®. Additional details on the control limits of the copper DBI® CMP including accommodating the increased chemical susceptibility and mechanical softness of the copper are available to Ziptronix licensees [18].

The reliability results are from a very small sample size, but for a preliminary initial evaluation indicate good reliability. The data indicates a slight preference for higher temperature heat treatments, but the small number of failures and sample size are statistically inconclusive. Additional reliability evaluations are underway and will be reported elsewhere.

These copper DBI® results are the best reported to date and suitable for a number of applications, including those where low thermal budgets and copper BEOL foundry compatibility are required. A summary of these state-of-the art results, comparison to state-of-the art results achieved at Ziptronix for other types of DBI® [5-8] and availability for licensing are shown in Figure 8.

DBI® Metal	Gold	Nickel	Copper
Minimum Pitch (um)	1,000	1.5	10
Maximum # Yielded Serial Connections	1	1,000,000	72,500
Lowest Thermal Budget	< 50°C	300°C	125°C
Lowest Contact Resistance (Ohm)		< 0.05	< 0.05
Lowest Contact Resistivity (Ohm/um^2)		< 0.5	< 0.45
Dual Damascene Integration			Yes
Barrier Layer Integration			Yes
Reliability		Good	Good
Licensing Availability	Ziptronix	Ziptronix	Ziptronix

Figure 8 – Performance and availability of different types of DBI® technology.

Conclusions

A copper DBI® technology has been developed that leverages foundry standard copper dual damascene and Ziptronix low temperature, high direct or non-adhesive oxide bond strength technologies to achieve scalable, very low CoO, 3D interconnects with minimum foundry adoption barrier. Results achieved include 100% operable arrays of 72,500 3D copper DBI® interconnections on a 25 micron pitch with a 125°C thermal budget and 10 micron pitch 3D copper DBI® interconnections with a 350°C thermal budget. DBI® contact resistance and resistivity achieved are about 50 mohm / connection and < 0.45 ohm/um^2, respectively, using 4 micron diameter Cu DBI® plugs and a TiW barrier layer. Preliminary reliability results include bare die that pass temperature cycling and HAST JEDEC tests. The copper DBI® technology is available for licensing and evaluation for volume semiconductor manufacturing.

References

[1] P. Enquist, “Direct Bond Interconnect Slashes Large-Die SOC Manufacturing Costs”, FSA forum, Fall 2006, p12.

[2] Q. Y. Tong, P. M. Enquist, A. S. Rose, U.S. Patent 6,962,835, “Method for Room Temperature Metal Direct Bonding”, Issued November 8, 2005.

[3] P. Enquist, “Room Temperature Direct Wafer Bonding for Three Dimensional Integrated Sensors”, Sensors and Materials, Vol. 17, No. 6, 2005, p. 307.

[4] C. Keast, B. Aull, J. Burns, C. Chen, J. Knecht, B. Tyrrell, K. Warner, B. Wheeler, V. Suntharalingam, P. Wyatt, and D. Yost, "Three-Dimensional Integrated Circuit Fabrication Technology for Advanced Focal Planes", MRS Symposium Fall 2006.

[5] Q. Y. Tong, "Room Temperature Metal Direct Bonding", Applied Physics Letters, 89, 1, 2006.

[6] P. Enquist, "High Density Direct Bond Interconnect (DBI™) Technology for Three Dimensional Integrated Circuit Applications", Fall MRS, 2006.

[7] P. Enquist, "Direct Bonding Processes for 3-D Integration", Handbook of 3D Integration, Vol 2, Chapter 11, 2008, p.487.

[8] P. Enquist, "Scalability and Low Cost of Ownership Advantages of Direct Bond Interconnect (DBI®) as Drivers for Volume Commercialization of 3-D Integration Architectures and Applications", Mater. Res. Soc. Symp. Proc. Vol. 1112, 2009, p.33.

[9] P. Gueguen, L.D. Cioccia, J.P. Gonchond, P.Gergaud, M. Rivoire, D. Scevola, M. Zussy, D. Lafond, L. Clavelier, "3D Vertical Interconnects by Copper Direct Bonding", Mater. Res. Soc. Symp. Proc. Vol. 1112, 2009, p.81.

[10] Yole, "3DIC Report", 2007 Edition, Revised August 15, 2008.

[11] Q.-Y. Tong, G. Fountain, and P. Enquist, US patent 6,902,987, "Method for Low Temperature Bonding and Bonded Structure", June 7, 2005.

[12] Q.-Y. Tong, G. Fountain, and P. Enquist, US patent 7,041,078, "Method for Low Temperature Bonding and Bonded Structure", May 9, 2006.

[13] Q.-Y. Tong, US patent 7,109,092, "Method of Room Temperature Covalent Bonding", September 19, 2006.

[14] Q.-Y. Tong, G. Fountain, and P. Enquist, US patent 7,335,572, "Method for Low Temperature Bonding and Bonded Structure", February 26, 2008.

[15] Q.-Y. Tong, US patent 7,335,996, "Method of Room Temperature Covalent Bonding", February 26, 2008.

[16] Q.-Y. Tong, G. Fountain, and P. Enquist, US patent 7,387,994, "Method for Low Temperature Bonding and Bonded Structure", June 17, 2008.

[17] Q.-Y. Tong, G. Fountain, and P. Enquist, US patent 7,553,744, "Method for Low Temperature Bonding and Bonded Structure", June 30 2009.

[18] www.ziptronix.com

[19] H. Nakajima, Packaging Summit Panel, Semicon, 2009.

[20] J. Eischen, private communication.